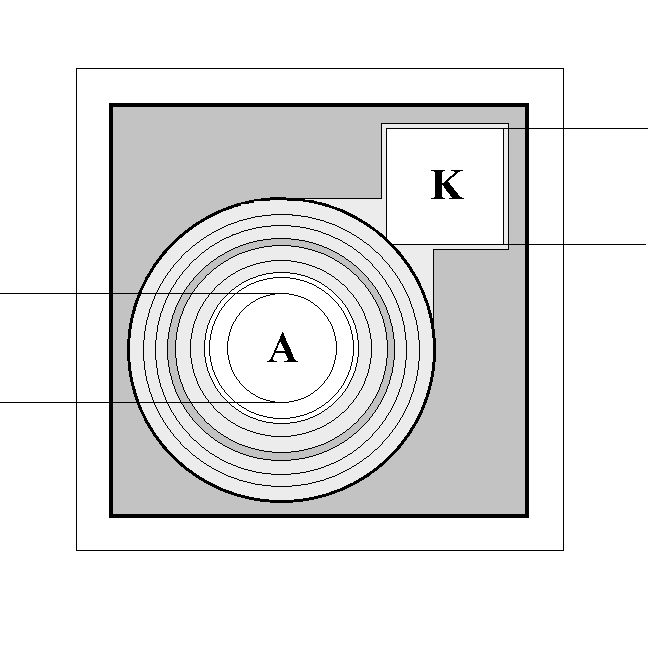
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.020”**

**.020”**



**.004”**

**.004”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Cathode**

**Mask Ref: KBA**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 8/26/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .008” P/N: 1N4148**

**DG 10.1.2**

#### Rev B, 7/19/02